1. GENERAL DESCRIPTION

The SENIS® 3DHALL sensor SENM3Dx is a CMOS integrated magnetic field sensor that allows the acquisition of all three magnetic-field components (Bx, By and Bz) at the same time and at the same spot. The sensor incorporates three groups of mutually orthogonal Hall-effect elements (one horizontal and two vertical) with biasing circuits and amplifiers for each of them. The integrated Hall elements are very compact and occupy a small area of about 100 x 100 μm^2. This allows for very high spatial resolution of the sensor. The applied CMOS technology enables high precision in the fabrication of the vertical and horizontal Hall elements, which gives high angular accuracy (orthogonality) of the three measurement axis. The application of the spinning-current technique in the biasing of the Hall elements significantly suppresses offset, low-frequency noise, and the planar Hall effect. The sensor provides high analog bandwidth from DC to 300kHz. A built-in temperature sensor allows to measure the current chip temperature at the field sensitive volume.

FEATURES:	TYPICAL APPLICATIONS:
▪ Real 3D magnetic-field measurement with the possibility to select the active sensitivity axis; any one, two or all three axis at the same time ▪ Analog, PWM and SPI (5V) digital interface ▪ High magnetic field resolution: 1 µT ▪ Field sensitive volume: 100 x 100 x 10 μm^3 ▪ Selectable measurement ranges: 30 mT to 4 T ▪ High analog frequency bandwidth: DC to 300 kHz ▪ Built-in temperature sensor ▪ On-chip correction of sensitivity, offset, noise and temperature drift, parametrizable in EEPROM ▪ Adjustable signal conditioning individually for each Hall sensor, Bx, By and Bz ▪ Programmable threshold comparator for each channel, enabling a signal level detection feature	▪ 3D Positioning sensor, linear and angular for joysticks, angle sensor ▪ 1D, 2D, 3D Proximity sensor ▪ Current sensor with any axis and selectable ranges ▪ Magnetometry, multi-probe measurement set-ups i.e. array of sensors

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

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PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

3. PACKAGE INFORMATION

The non-magnetic QFN28 package has a lead frame made of copper and the body material is a semiconductor molding epoxy. Contact SENIS for details.

3.1 Dimensions

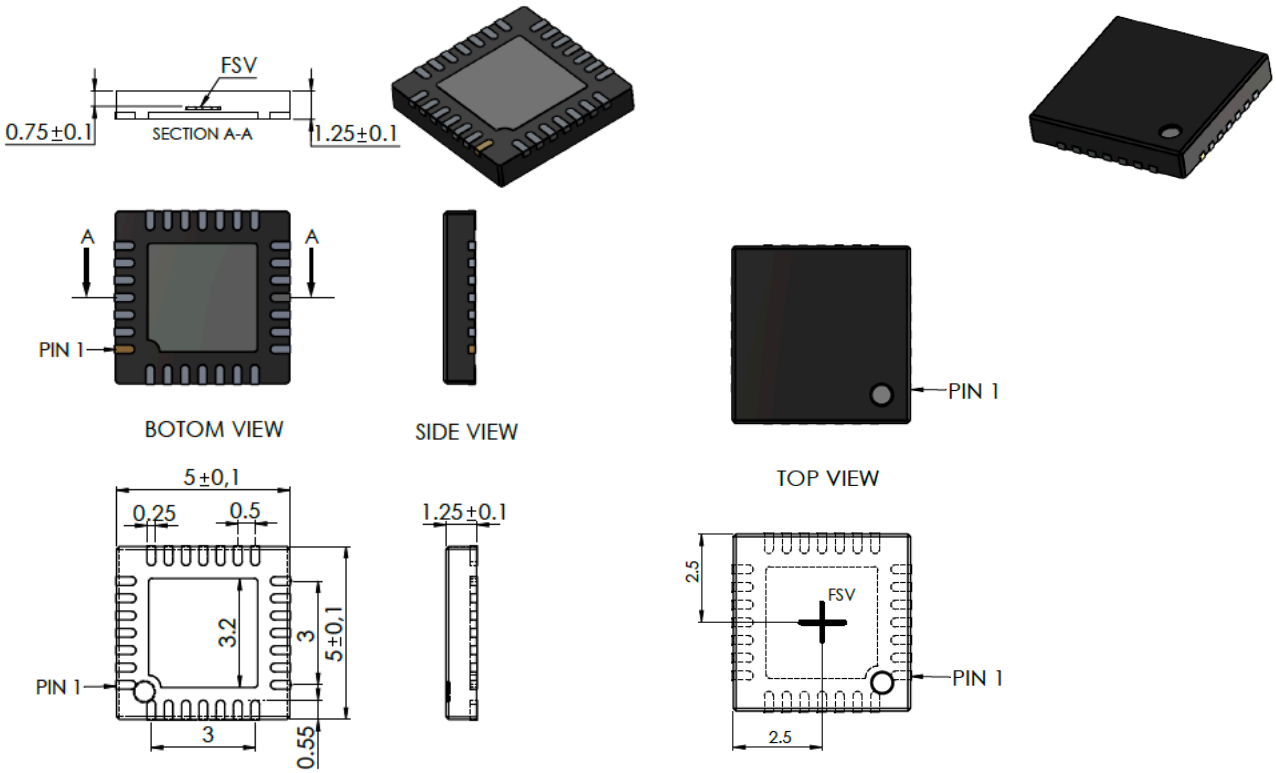

Figure 1: Dimensions of QFN 5x5 mm² package with 28 pads. The field sensitive volume (FSV) is located at the center of the package. Not to scale

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FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

3.2 Pinout

Pin #	Symbol	Type	Direction	Description.
1	-	-		Not connected
2	VCM	Ground	Power	Virtual ground (+2.45V); bypass capacitor 100 nF optional
3	VREF	Analog	Out	Bandgap reference voltage (+1.25V); bypass capacitor 100 nF to GNDA
4	MCLK	Digital	In	SPI Master Clock
5	MOSI	Digital	In	SPI Master Out Slave In
6	MISO	Digital	Out	SPI Master In Slave Out
7	-	-	-	Not connected
8	-	-	-	Not connected
9	SSB	Digital	In	SPI Chip (Slave) Select; active-low
10	TEST_EN	Digital	In	For internal use only; do not connect
11	TEST_DMUX	Digital	Out	For internal use only; do not connect
12	VDD	Supply	Power	Internal regulated digital supply voltage (3.3V); bypass capacitor 100 nF to GNDD
13	GNDD	Supply	Power	Ground digital
14	-	-	-	Not connected
15	-	-	-	Not connected
16	YD	Digital	Out	Magnetic field component By as PWM or comparator output
17	XD	Digital	Out	Magnetic field component Bx as PWM or comparator output
18	ZD	Digital	Out	Magnetic field component Bz as PWM or comparator output
19	VCCA	Supply	Power	Internal regulated analog supply voltage (4.5V); bypass capacitor 100 nF to GNDA
20	VCC	Supply	Power	Main supply voltage (+5V)
21	-	-	-	Not connected
22	-	-	-	Not connected
23	YA	Analog	Out	By field component voltage output
24	XA	Analog	Out	Bx field component voltage output
25	ZA	Analog	Out	Bz field component voltage output
26	TA	Analog	Out	Sensor chip temperature voltage output
27	GNDA	Supply	Power	Ground analog
28	-	-	-	Not connected

Table 1: SENM3Dx Pin List

PHONE +41 43 205 26 37
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3.3 Sensitivity Vectors

Figure 2 shows the QFN28 package and corresponding magnetic sensitivity axis with respect to pin 1.

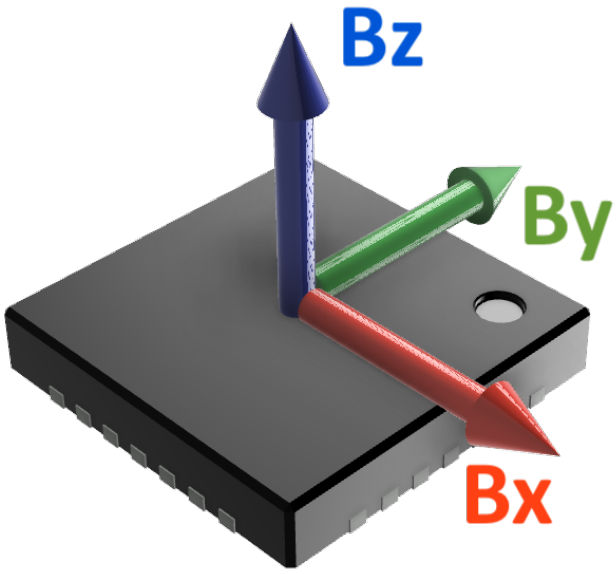

Figure 2: Magnetic Axis Orientation.

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4. BLOCK DIAGRAM

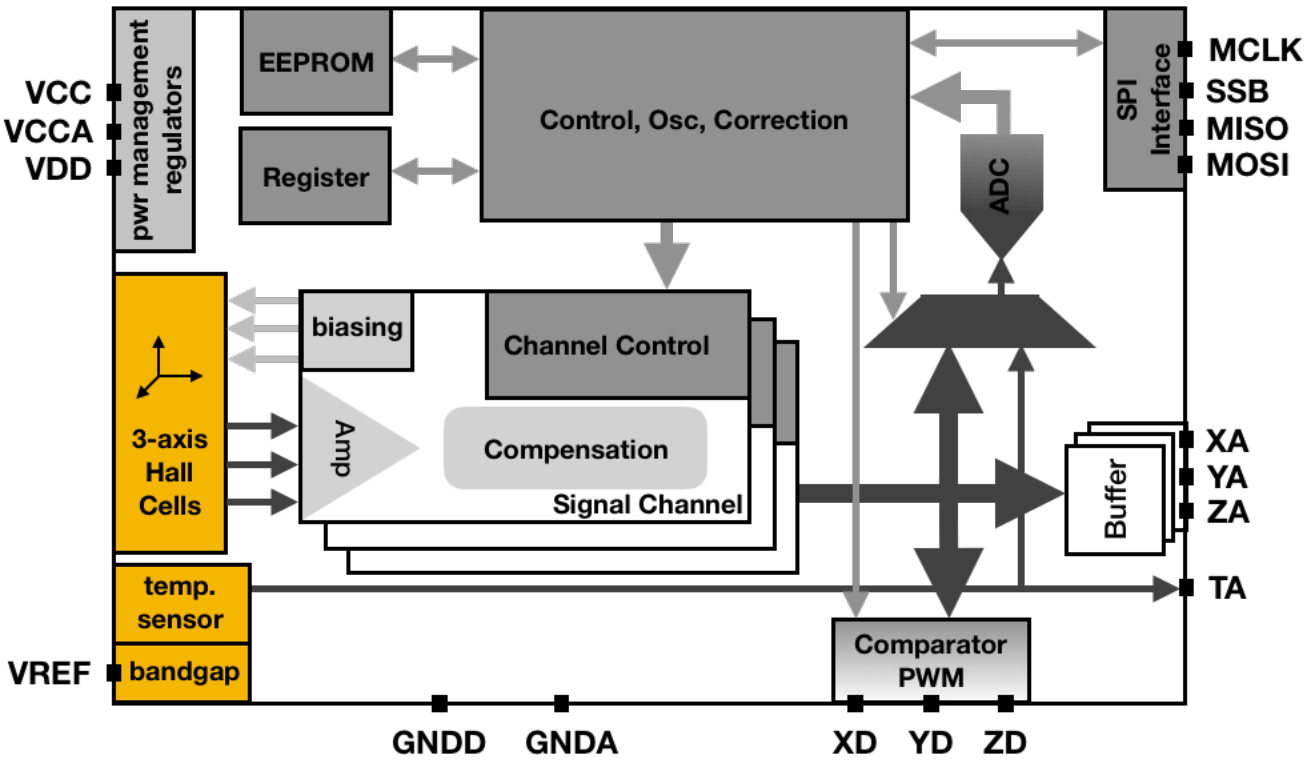

Figure 3: Block diagram of SENM3Dx

5. ABSOLUTE MAXIMUM RATINGS

Parameter, Unit	Min. Rating	Max. Rating
Power supply voltage VCC [V]	-	7
Digital input voltage [V]	-0.3	VCC+0.3
Shorted output current [mA]	-50	50
Storage temperature [°C]	-50	150
Operation temperature [°C]	-40	125
Lead temperature, 10s soldering [°C]	-	220
ESD protection at inputs, HBM [kV]	-2	2
Magnetic Field [T]	-6	6

Table 2: Absolute Maximal Ratings

Note that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

6. GLOSSARY OF TERMS

Name, Acronym	Description
ADC	Analog-to-Digital Converter
BW	Band Width
CPOL	Clock Polarity
CPHA	Clock Phase
DAC	Digital-to-Analog Converter
ENOB	Effective Number of Bits
EEPROM, E^2PROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FSV	Field Sensitive Volume
HBM	Human-body model
kSPS	1000 Samples per second
MCLK	Master Clock
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Byte
NSD	Noise Spectral Density
NVM	Non-Volatile Memory
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SSB	Slave Select Low-Active

Table 3: Glossary of terms

7. MAGNETIC AND ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the given specifications and characteristics are typical values and apply for room temperature (23°C) and after a device warm up time of 15 minutes. VCC=5 V, Hall element bias current of 3.5 mA in four phase spinning.

Parameter, Unit	Typical Value
Power supply voltage VCC [V]	5
Current consumption [mA]	< 40
Analog voltage regulator output [V]	4.5
Digital voltage regulator output [V]	3.2
Reference voltage output [V]	1.2
Common voltage output [V]	2.4
Analog output range to GND [V]	0.05 - 4.40
Operating temperature [°C]	-40 to +125

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FAX +41 43 205 26 38
E-MAIL info@senis.ch
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6340 Baar, Switzerland

Field Sensitive Volume [µm^3]	100 x 100 x 10
Crosstalk between channels	<0.2 %
Output resistance	10kOhm //2nF
Output current capability	20 mA
Oscillator frequency [MHz]	20
Spinning frequency	500 kHz, 4 phases
Hall element biasing current [mA]	4.5 mA
3dB Frequency Bandwidth	DC – 300 kHz
Measurable magnetic flux density [T]	±6

Table 4: Typical electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
High level input voltage	V_{IH}	3	3.5	5.3	V	VCC=5V
Low level input voltage	V_{IL}	1	1.5	2	V	VCC=5V
High level output voltage	V_{OH}			VCC-0.3	V	Iout=4mA
Low level output voltage	V_{OL}			0.3	V	Iout=4mA
Input leakage current	I_{LEAK}	-10		10	pA	
Input capacitance	C_{IN}			5	pF	

Table 5: Digital I/O characteristics

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

Range Name	Measurement Range [mT] Min./Max.
30 mT	-30/+40
60 mT	-50/+70
500 mT	-440/+600
4 T	-3400/+4000

Table 6: Selectable Main Magnetic Field Measurement Ranges. See for Table 21 Details.

Non-linearity of the sensor signal is < 1% for all axis over the full signal range.

Sensitivity to DC magnetic field	Value for specified axis		
	Bx	**By**	**Bz**
Range			Sensitivity [V/T]
30 mT	150	150	150
60 mT	75	75	75
500 mT	7.5	7.5	7.5
4 T	0.7	0.7	0.7

Table 7: Sensor Sensitivity Overview

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FAX +41 43 205 26 38
E-MAIL info@senis.ch
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Neuhofstrasse 5a
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Zero Magnetic Field Offsets	Value for specified axis		
	Bx	**By**	**Bz**
Range			Output voltage [mV]
30 mT	*-170*	*350*	*104*
60 mT	*-108*	*170*	*-103*
500 mT	-16	15	-12
4 T	-11	-1.4	-12
Range			Corresponding Magnetic Field [mT]
30 mT	*-1.1*	*2.3*	*0.7*
60 mT	*-1.4*	*2.2*	*-1.3*
500 mT	-2.1	2.0	-1.6
4 T	-15.7	-2.0	-17.1

Table 8: Uncorrected Zero Magnetic Field Offsets

Noise Spectral Densities	Value for specified axis		
	Bx	**By**	**Bz**
Range			Voltage noise NSD @ f > 10 Hz (white noise), [µV/$\sqrt{Hz}$]
30 mT	23.0	23.0	22.0
60 mT	7.5	13.0	14.0
500 mT	1.8	1.6	1.7
4 T	*1.0*	*1.0*	*1.1*
Range			Corresponding Magnetic Field NSD @ f > 10 Hz (white noise), [µV/$\sqrt{Hz}$]
30 mT	*0.37*	*0.36*	*0.37*
60 mT	*0.22*	*0.37*	*0.42*
500 mT	*0.43*	*0.38*	*0.41*
4 T	*1.53*	*1.44*	*1.80*

Table 9: Input Referred, Equivalent White Noise Specification of the Sensor

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

Parameter for Analog & Digital Output	Value for specified axis		
	Bx	**By**	**Bz**
Analog output voltage range referenced to the GND [V]	0.125 - 4.380		
Temperature Coeff. of Sensitivity @ Temperature range 25±10°C [ppm/°C]		<100	
Range Temperature Coeff. of Offset (@B = 0T, @ Temp. range 15-45°C) [mV/°C]			
30 mT	*-0.640*	*3.010*	*-0.040*
60 mT	-0.330	*1.350*	-0.026
500 mT	-0.040	0.150	-0.003
4 T	0.010	0.020	-0.003
Range Corresponding digital values (@B = 0T, @ Temp. range 15-45°C) [LSB/°C]			
30 mT	26.00	29.00	-0.20
60 mT	15.00	17.00	-0.24
500 mT	1.60	2.00	0.18
4 T	1.10	0.17	0.02
Range Offset voltage fluctuation & drift (peak-to-peak value) (Δt = 0.05s, t = 100s) [µVrms]			
30 mT	116.0	130.0	320.0
60 mT	146.0	90.0	117.0
500 mT	11.0	12.3	12.0
4 T	11.0	8.7	12.0
Range;Corresponding field offset fluctuation & drift (peak-to-peak value) (Δt = 0.05s, t = 100s) [µTrms]			
30 mT	0.7	0.8	2.1
60 mT	1.9	1.2	1.5
500 mT	1.4	1.6	1.6
4 T	15.0	12.0	17.0

Table 10: Temperature Coefficients and Fluctuations. Note that the Temperature Coefficients can be compensated.

ADC	
ADC resolution [bit]	16
ADC sample rate [kSPS]	8
Conversion [µV/LSB]	60

Table 11: ADC Specification

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Temperature sensor, analog and digital out	
Output voltage TA @0°C [V]	1.65
Sensitivity of TA, Range 15-40°C, [mV/°C]	10.30
Digital Temperature Reading Sensitivity, range 15-40°C [LSB/°C]	168
Digital Temperature Reading @0°C [LSB]	19913
Temperature sensor accuracy [°C]	< 0.1

Table 12: Temperature Sensor Specification

PWM Digital Output	
PWM resolution (ENOB) [bit]	12 - 16
PWM output frequency range [Hz]	4777-298
Response time [ms]	0.5
Jitter [LSB]	1
Output voltage high [V]	4.6
Output voltage low [V]	0.4
Rising edge slew rate [V/µs]	2
Falling edge slew rate [V/µs]	2

Table 13: PWM Characteristics and Properties (details in chapter 9.2.2)

The analog output voltages XA, YA and ZA (<X,Y,Z>*A*) are given by

<X,Y,Z>A = (Iin * Gain*(Vin-THRES_<X,Y,Z>))^2 + (Gain * (Vin-THRES_<X,Y,Z>)) * Iin + Gain * Vin,

where Iin denotes an internal control signal for linearity correction, THRES_<X,Y,Z> is the comparator threshold voltage setting (see chapter 9.2.5) of the respective channel, Gain is the amplification of the entire signal chain from the Hall element itself to the output (see chapter 9.2.6) and Vin is the voltage drop across the Hall element.

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

8. SPI INTERFACE

The SENM3Dx is compatible with SPI mode 1, active-low chip (slave) select and fixed 8-bit length. This means, that clock polarity (CPOL) equals '0' and clock phase (CPHA) equals '1', i.e. data will be transferred on the falling edge of MCLK, while '0' is the idle or inactive state of MCLK. The SENM3Dx behaves always as slave of the SPI communication interface and 5V signal levels (see Table 5).

Parameter	Symbol	Min.	Max.	Unit
Clock period	Tcp	40		ns
Setup time from SSB low to MCLK high	Tsc	100		ns
Hold time from SSB high to MCLK low	Thc	100		ns
MOSI setup time to MCLK (1->0)	Tsi	5		ns
MOSI Hold time to MCLK (1->0)	Thi	0		ns
MISO propagation time from tri-state to logic (SSB=0)	Ttr2d		10	ns
MISO propagation time from logic to tri-state (SSB=1)	Td2tr		10	ns
MISO propagation time from MCLK (1->0)	Tdo		8	ns

Table 14: SPI Timing Parameter

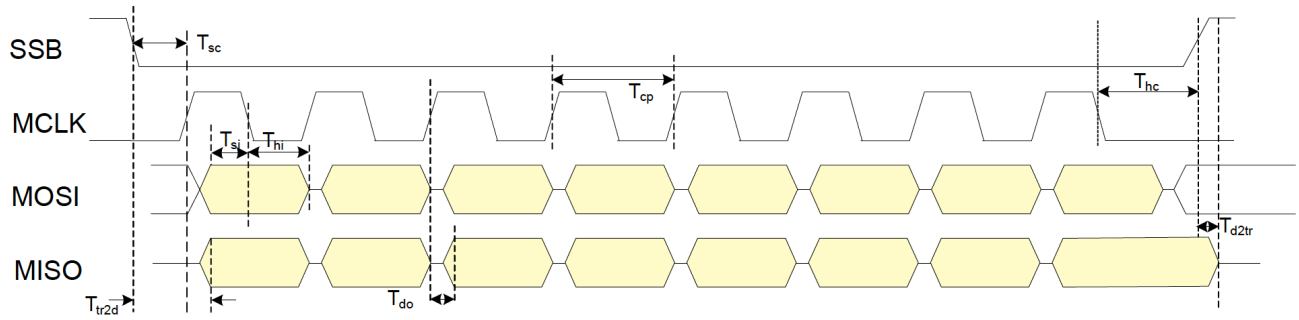

Figure 4: SPI Timing Parameter Definitions

8.1 Register Read/Write Access

The access to the SPI interface is memory mapped and implemented as follows:
The first byte (8 bits) sent from the master (host; MOSI) represents a command word and includes a direction control bit (most significant bit): '0' for read and '1' for write access followed by a 7-bit address which is zero (i.e. in hex format 0x00) for the register memory space (Figure **5**). The second byte represents the 8-bit address (ADD) to read or write.

8.1.1 Register Read Access

For a register read operation, the SENM3Dx responds (MISO) - by sending the most significant bit first - the data byte (Data[ADD]) from the provided address. The addressed data is available and valid after one byte delay,

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

following the address byte. Multiple bytes can be read sequentially - from the provided address on - in a single SPI frame, which closes with the rising SSB signal.

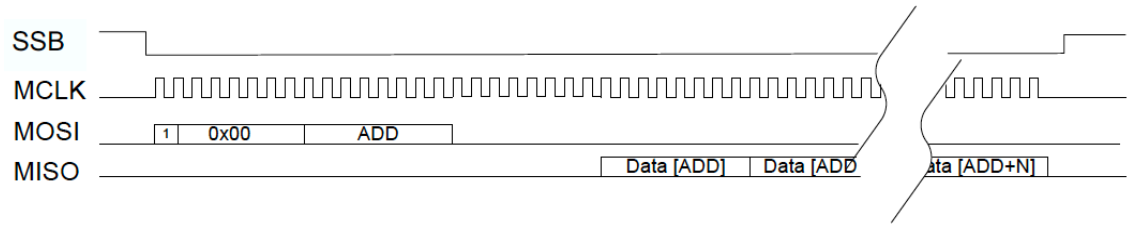

Figure 5: SPI Communication for Register Read Access Timing Diagram

8.1.2 Register Write Access

The register write access starts with a leading (MSB) '0', followed by 7 zero bits to conclude the first byte sent from the host (*Figure 6*). The second byte contains the write address, followed by the data to write byte. Again, as mentioned for the register read access, also the write operation may be performed sequentially within one SPI frame for incremental addresses. Note that during the write process the MISO signal is unused, thus kept at '0'.

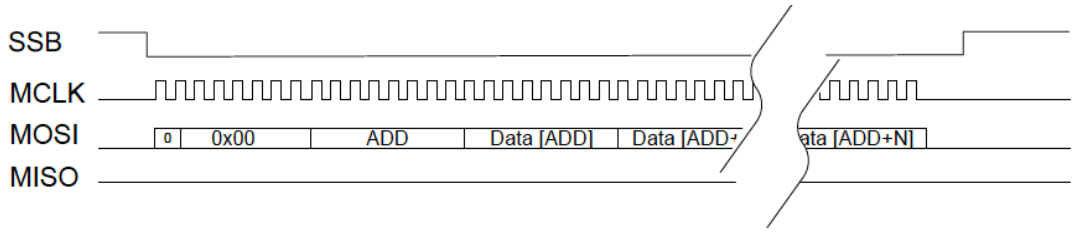

Figure 6: SPI Communication for Register Write Access Timing Diagram

8.2 EEPROM Read/Write Access

The internal 256 x 8bit EEPROM is a non-volatile memory which holds initialization and calibration data as well as gain dependent settings and the definition of internal measurement sequences. To change the address space from register to EEPROM access, the last bit of the first byte has to be set to '1'. Furthermore, the command word again includes the direction control bit 0 for read and '1' for write access. However, the read and write EEPROM access is somewhat different from the register access detailed before, since read/write operations return a special key (0xA5) via MISO (*Figure 7 and Figure 8)* to acknowledge the transfer and only single byte transfers per SPI frame are supported (i.e. no sequential read or write access possible).

8.2.1 EEPROM Read Access

For an EEPROM read operation, the ASIC responds with a special acknowledge byte 0xA5 followed by the addressed data. Depending on the ratio between the internal clock and the SPI clock frequency, this can happen at the earliest at the second byte following the command byte. Data sent by the SPI master (host) after the expected data byte will be disregarded. The master should therefore keep the SPI frame active until the acknowledge and data is received to ensure data integrity.

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E-MAIL info@senis.ch
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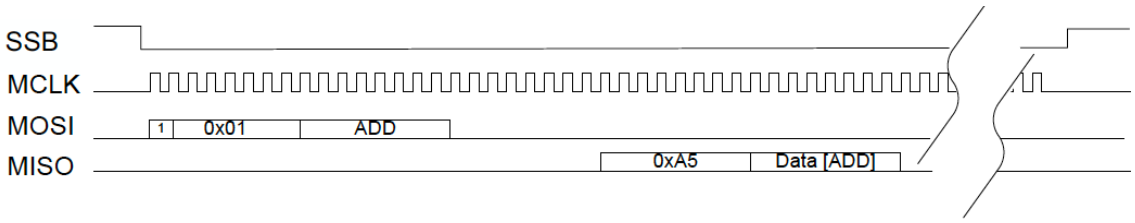

Figure 7: SPI Communication for EEPROM Read Access Timing Diagram

8.2.2 EEPROM Write Access

The EEPROM write access lasts nominally 12 ms for programming one byte. The ASIC responds again with the acknowledge byte 0xA5 once the write operation is successfully completed. The SPI master (host) should leave the SPI frame active until the acknowledge byte is received, otherwise EEPROM data consistency cannot be guaranteed.

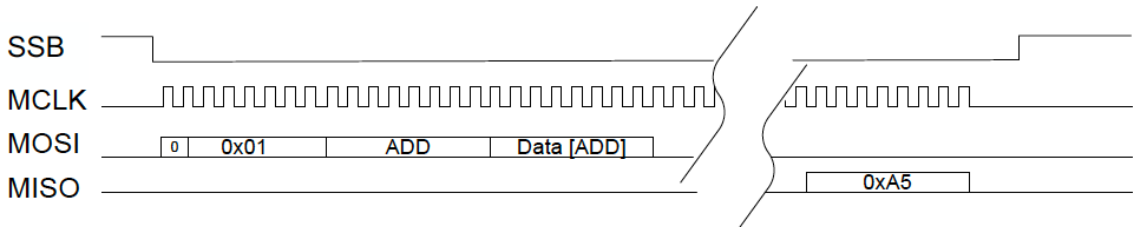

Figure 8: SPI Communication for EEPROM Write Access Timing Diagram

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

9. REGISTERS

9.1 Register Map

Table 15 shows a list of all user relevant registers. Register addresses which are not shown in the list (i.e. 0x3E, 0x40 to 0xFF) must not be written, since they contain data essential for the ASIC operation. The default values detailed in the list are loaded to the registers at power-up if the EEPROM data is not activated (i.e. valid check sum and key present). Note that LSB and MSB are used here for least and most significant byte respectively. Register REG_0 to REG_7 control the spinning current state machine and the default values are the best possible settings, thus they should not be changed.

Register ID	Address	Default value	Mode	Meaning	EEPROM location	Gain dependent
REG_0	0x00	16	R/W	Do not change	Yes	No
REG_1	0x01	18	R/W	Do not change	Yes	No
REG_2	0x02	19	R/W	Do not change	Yes	No
REG_3	0x03	17	R/W	Do not change	Yes	No
REG_4	0x04	57	R/W	Do not change	Yes	No
REG_5	0x05	60	R/W	Do not change	Yes	No
REG_6	0x06	0	R/W	Do not change	Yes	No
REG_7	0x07	0	R/W	Do not change	Yes	No
PWM_CTRL	0x08	0	R/W	PWM scaling factor	Yes	No
CHANNEL_CTRL	0x09	15	R/W	Channel enable and digital output selection.	Yes	No
OSC trim	0x0A	32	R/W	Oscillator trim data.	Yes	No
THRES_Y	0x0B	0	R/W	Channel Y threshold control.	Yes	No
THRES_X	0x0C	0	R/W	Channel X threshold control.	Yes	No
THRES_Z	0x0D	0	R/W	Channel Z threshold control.	Yes	No
G_CTRL_Y	0x0E	2	R/W	Pre-amplifier gain control Y.	Partial	-
G_CTRL_X	0x0F	2	R/W	Pre-amplifier gain control X.	Partial	-
G_CTRL_Z	0x10	2	R/W	Pre-amplifier gain control Z.	Partial	-
DAC_Y	0x11	8	R/W	Hall element X bias current control	Yes	Yes
DAC_X	0x12	8	R/W	Hall element Y bias current control	Yes	Yes
DAC_Z	0x13	8	R/W	Hall element Z bias current control	Yes	Yes
SENS_Y	0x14	0	R/W	Channel Y linearity control.	Yes	Yes
SENS_X	0x15	0	R/W	Channel X linearity control.	Yes	Yes
SENS_Z	0x16	0	R/W	Channel Z linearity control.	Yes	Yes
SENS_TC_Y	0x17	0	R/W	Channel Y sensitivity temp. coef. Control.	Yes	Yes
SENS_TC_X	0x18	0	R/W	Channel X sensitivity temp. coef. Control.	Yes	Yes

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

SENS_TC_Z	0x19	0	R/W	Channel Z sensitivity temp. coef. Control.	Yes	Yes
OFFSET_Y	0x1A	0	R/W	Channel Y offset control.	Yes	Yes
OFFSET_X	0x1B	0	R/W	Channel X offset control.	Yes	Yes
OFFSET_Z	0x1C	0	R/W	Channel Z offset control.	Yes	Yes
OFFSET_TC_Y	0x1D	0	R/W	Channel Y offset temp. coef. Control.	Yes	Yes
OFFSET_TC_X	0x1E	0	R/W	Channel X offset temp. coef. Control.	Yes	Yes
OFFSET_TC_Z	0x1F	0	R/W	Channel Z offset temp. coef. Control.	Yes	Yes
STATUS	0x3F	-	R	Status byte	No	-
ADC_DATAYL	0x40	-	R	ADC readout data (LSB) Y channel	No	-
ADC_DATAYH	0x41	-	R	ADC readout data (MSB) Y channel	No	-
ADC_DATAXL	0x42	-	R	ADC readout data (LSB) X channel	No	-
ADC_DATAXH	0x43	-	R	ADC readout data (MSB) X channel	No	-
ADC_DATAZL	0x44	-	R	ADC readout data (LSB) Z channel	No	-
ADC_DATAZH	0x45	-	R	ADC readout data (MSB) Z channel	No	-
ADC_DATATL	0x46	-	R	ADC readout data (LSB) Temperature	No	-
ADC_DATATH	0x47	-	R	ADC readout data (MSB) Temperature	No	-

Table 15: Overview Register Map and Settings

9.2 Register Content

9.2.1 Spinning Phase Settings

The sequencer is configured by register values from address 0x00 to 0x07. The user should not change those values and if the data loading from EEPROM is activated, the default values shown in Table 15 have to be used.

Register ID	Address	Mode	Bits	Meaning	Default
REG_0 to REG_7	0x00 to 0x07	R/W	7:0	Do not change	Table 15

Table 16: Registers for Hall Element Spinning Current Setting

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

9.2.2 Pulse Width Modulation Settings

Figure 9 shows the timing diagram of the PWM cycle. A parameter in the configuration register PWM_CTRL (defined below) scales the entire waveform.

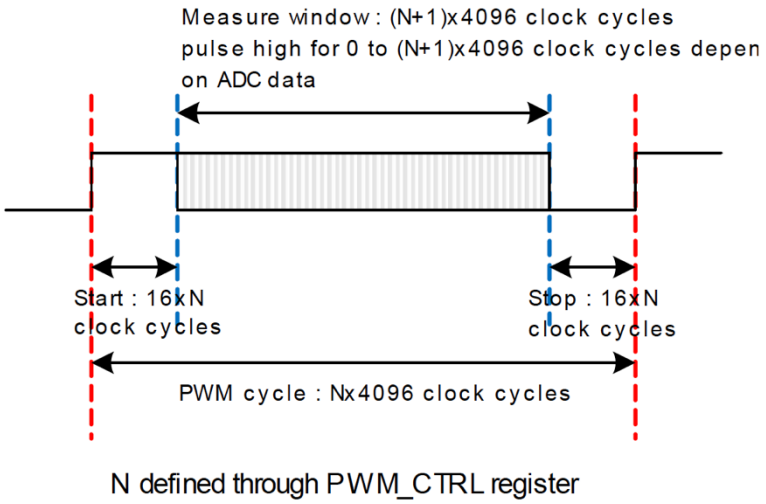

Figure 9: PWM Timing Diagram

Register ID	Address	Mode	Bits	Meaning	Default
PWM_CTRL	0x08	R/W	2:0	Scaling of PWM cycle (20 MHz clock) 0 -> 4.845 kHz 1 -> 2.42 kHz 2 -> 1.21 kHz 3 -> 605 Hz 4 -> 302 Hz 7-5 -> Invalid (processed as 4)[1]	0
			7:3	Reserved	0

Table 17: Register Settings for PWM Interface

9.2.3 Channel Control Settings and ADC Data

The ADC scan rate is always 8 kSPS, so if only one magnetic field measurement channel and the temperature channel are enabled, the conversion rate will be 8 kSPS/2 = 4 kSPS. In case a channel is disabled, the associated output data will be read as 0 via SPI and the power will be turned off for this channel (which includes the respective DAC for this channel).
Note that the ADC data should be read at once and sequentially, i.e. one SPI transfer for 4 x 2 bytes starting from address
0x40.

[1] *: If the register value is 0 (fastest speed), only the 12 MSB of the ADC data will be used for PWM. Any increment from that will use one additional bit. For the largest setting (4; slowest PWM cycle) all 16 bits will be used.*

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

Register ID	Address	Mode	Bits	Meaning	Default
CHANNEL_CTRL	0x09	R/W	0	1= channel Y enabled 0 = channel Y disabled	1
			1	1= channel X enabled 0 = channel X disabled	1
			2	1= channel Z enabled 0 = channel Z disabled	1
			3	1= Temperature sensor enabled 0 = Temperature sensor disabled	1
			4	1= PWM enabled for channel Y on YD 0= Comparator output routed through YD	0
			5	1= PWM enabled for channel X on XD 0= Comparator output routed through XD	0
			6	1= PWM enabled for channel Z on ZD 0= Comparator output routed through ZD	0
			7	Two phases enable	0
ADC_DATAYL	0x40	R	7:0	LSB Data from the ADC converter – channel Y	-
ADC_DATAYH	0x41	R	15:8	MSB Data from the ADC converter – channel Y	-
ADC_DATAXL	0x42	R	7:0	LSB Data from the ADC converter – channel X	-
ADC_DATAXH	0x43	R	15:8	MSB Data from the ADC converter – channel X	-
ADC_DATAZL	0x44	R	7:0	LSB Data from the ADC converter – channel Z	-
ADC_DATAZH	0x45	R	15:8	MSB Data from the ADC converter – channel Z	-
ADC_DATATL	0x46	R	7:0	LSB Data from the ADC converter – Temp	-
ADC_DATATH	0x47	R	15:8	MSB Data from the ADC converter – Temp	-

Table 18: Register Setting for Channel Control

9.2.4 Clock Frequency Settings

The nominal 20 MHz clock may be trimmed by the user within the range of 10 to 30 MHz.

Register ID	Address	Mode	Bits	Meaning	Default
OSC trim	0x0A	R/W	5:0	Trim frequency ~300kHz /step	32
			7:6	Reserved	0

Table 19: Register for Oscillator Trimming Settings

9.2.5 Comparator Threshold Settings

Each channel includes a comparator with hysteresis and programmable threshold value to give a '1' at the output, if the signal level is above the threshold. The output of the comparator is shared with the PWM interface and one may be selected. These threshold values also used for linear and quadratic correction of the measured Hall voltage (see chapter 7).

Register ID	Address	Mode	Bits	Meaning	Default
THRES_Y	0x0B	R/W	6:0	Full scale 0-1.2V, 9.4mV/step	0
THRES_X	0x0C	R/W	6:0	Full scale 0-1.2V, 9.4mV/step	0
THRES_Z	0x0D	R/W	6:0	Full scale 0-1.2V, 9.4mV/step	0

Table 20: Registers for Comparator Threshold Settings

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

9.2.6 Hall Element Voltage Gain Settings

The gain control registers in Table 23 are used to select the gain of the entire signal chain, reaching from the Hall elements to the analog outputs. Gain values range from 7.5 to 3000 and two selection methods (2 and 4 bits) are available. Table 22 shows the main (default) selection method for the gain value with 2 bits, thus there are four possibilities.

7.5	75
15	150
30	300
75	750
150	1500
300	3000

gain selection 1: 4 bits
gain selection 0: 2 bits

Table 21: Possible Gain Value Selection for Signal Channel

Voltage Gain [V/V]	Measurement Range [mT] Min./Max.
3000	-30/+40
1500	-50/+70
150	-440/+600
15	-3400/+4000

Table 22: Gain Value Selection and Associated Measurement Ranges

Register ID	Address	Mode	Bits	Meaning	Default
G_CTRL_Y G_CTRL_X G_CTRL_Z	0x0E 0x0F 0x10	R/W	1:0	Gain selection 00 -> Gain 3000 01 -> Gain 1500 10 -> Gain 150 11 -> Gain 15	2
			3	Gain selection method 0 -> Gain is controlled by bit 1:0 1 -> Gain is controlled by bit 7:4	0
			4	G_PRE: Gain selection for Preamp 1 -> 1V/V 0 -> 10V/V	0
			6:5	G_MAIN: Gain selection of the main amplifier 11 -> 2.5V/V 01 -> 5V/V 00 -> 10 V/V	0
			7	G_REC: Gain selection of rectifier (include gain of output stage) 1 -> 3V/V 0 -> 30V/V	0

Table 23: Register for Signal Channel Gain Settings

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

9.2.7 Current Source Settings For Hall Elements Bias

The current source generating the bias current for each Hall element is implemented as 8-bit DAC. This DAC allows the user to fine tune the sensitivity of the Hall sensor.

Register ID	Address	Mode	Bits	Meaning	Default
DAC_Y	0x11	R/W	5:0	Control current source of the Y axis Hall sensor 0 -> 500uA .. 63 -> 8mA	8
			7:6	Reserved	0
DAC_X	0x12	R/W	5:0	Control current source of the X axis Hall sensor 0 -> 500uA .. 63 -> 8mA	8
			7:6	Reserved	0
DAC_Z	0x13	R/W	5:0	Control current source of the Z axis Hall sensor 0 -> 500uA .. 63 -> 8mA	8
			7:6	Reserved	0

Table 24: Register Settings for Biasing Hall Elements

9.2.8 Linearity Compensation Settings For Hall Elements

Since the Hall sensor may exhibit some non-linearity at large magnetic fields, a linearity compensation circuit is added into the Hall current sensor to compensate for this effect. This circuit adjusts the bias current into the Hall element.

Register ID	Address	Mode	Bits	Meaning	Default
SENS_Y	0x14	R/W	6:0	Adjust Hall element bias current for sensitivity correction Iout= Iin *(1+ SENS_Y*3.9e^{-4})	0
			7	Reserved	0
SENS_X	0x15	R/W	6:0	Adjust Hall element bias current for sensitivity correction Iout= Iin *(1+ SENS_X*3.9e^{-4})	0
			7	Reserved	0
SENS_Z	0x16	R/W	6:0	Adjust Hall element bias current for sensitivity correction Iout= Iin *(1+ SENS_Z*3.9e^{-4})	0
			7	Reserved	0

Table 25: Register for Linear Sensitivity Correction

9.2.9 Temperature Compensation Settings For Hall Elements

The sensitivity of a Hall element depends on temperature and therefore needs to be compensated. The temperature compensation circuit can be programmed with a temperature coefficient changing from 400ppm/C to 3000ppm/C in 32 steps of 80ppm.

Register ID	Address	Mode	Bits	Meaning	Default
SENS_TC_Y	0x17	R/W	4:0	Adjust bias current to compensate for temperature effect on sensitivity Iout= Iin *(1+ SENS_TC_Y*(400e^{-6} + SENS_TC_Y*80e^{-6}))	0
			7:5	Reserved	0

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

Register ID	Address	Mode	Bits	Meaning	Default
SENS_TC_X	0x18	R/W	4:0	Adjust bias current to compensate for temperature effect on sensitivity Iout= Iin *(1+ SENS_TC_X*(400e^{-6} + SENS_TC_X*80e^{-6}))	0
			7:5	Reserved	0
SENS_TC_Z	0x19	R/W	4:0	Adjust bias current to compensate for temperature effect on sensitivity Iout= Iin *(1+ SENS_TC_Z*(400e^{-6} + SENS_TC_Z*80e^{-6}))	0
			7:5	Reserved	0

Table 26: Register for Correction of Sensitivity Temperature Coefficient

9.2.10 Offset Correction Settings For Hall Elements

If the Hall elements still show a DC offset voltage, even though there is the spinning current biasing method applied, there are three registers dedicated to compensate for it.

Register ID	Address	Mode	Bits	Meaning	Default
OFFSET_Y OFFSET_X OFFSET_Z	0x1A 0x1B 0x1C	R/W	6:0	Channel X,Y and Z offset adjustment 440µV/step	0
			7	Offset polarity control 0 -> positive offset 1 -> negative offset	0

Table 27: Register for Hall Element Offset Correction Settings

9.2.11 Temperature Coefficient Of Offset Correction Settings For Hall Elements

Again, the residual offset of the Hall element depends on temperature and this temperature coefficient can be corrected. Note that his correction should be applied after all other corrections (TC, linearity, etc.).

Register ID	Address	Mode	Bits	Meaning	Default
OFFSET_TC_Y OFFSET_TC_X OFFSET_TC_Z	0x1D 0x1E 0x1F	R/W	5:0	Temperature dependent offset compensation 0 -> no compensation 1 -> 6.25µV/C .. 63 -> 400µV/C	0
			6	Temperature polarity control 0 -> positive compensation 1 -> negative compensation	0
			7	Reserved	0

Table 28: Register for Temperature Coefficient of Hall Element Offset Correction Settings

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

9.2.12 Sensor Status Register

The status register includes various flags which reflect the current state of the ASIC and they are either updated at power-up, or dynamically (i.e. “on-the-fly”). Note that the comparator associated flags are valid only if the respective channel is enabled through the corresponding PWR_CTRL register (see 9.2.3).

Register ID	Address	Bits	Meaning	Flag update
STATUS	0x3F	0	EEPROM checksum error	Power-up
		1	EEPROM key invalid	Power-up
		2	Comparator status channel Y	Dynamic
		3	Comparator status channel X	Dynamic
		4	Comparator status channel Z	Dynamic
		5	Device busy When this bit is high, no EEPROM access should be performed, and no update of G_CTRL_... should be requested	Power-up and G_CTRL_... register update
		7:6	Not used	-

Table 29: ASIC Status Register

10. EEPROM MEMORY MAP

The ASIC is designed the way that gain independent settings are located in the EEPROM from address 0x100 to 0x10E (Table 31) and those that have to be adapted according to the chosen gain (Table 32). Since the data stored in the EEPROM reflect the respective settings in the registers (just named differently e.g. EREG_0 instead of REG_0), thus the details about their meaning is detailed in chapter 9.2. Note that for the settings in Table 32 only the 2 bit gain values stored in registers G_CTRL_X, G_CTRL_Y and G_CTRL_Z, are always used to read the calibration data from the EEPROM (see Table 21). The gain selection in the EEPROM EGain_sel (address 0x10E) is shown in Table 30.

E_Gain_sel (address 0x10E)							
7	6	5	4	3	2	1	0
-	-	Z Gain Selection		X Gain Selection		Y Gain Selection	

Table 30: Bits for Gain Selection in the EEPROM.

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

ID	Address
EREG_0	0x100
EREG_1	0x101
EREG_2	0x102
EREG_3	0x103
EREG_4	0x104
EREG_5	0x105
EREG_6	0x106
EREG_7	0x107
EPWM_CTRL	0x108
EChannel_Ctrl	0x109
OSC trim	0x10A
ETHRES_Y	0x10B
ETHRES_X	0x10C
ETHRES_Z	0x10D
EGain_sel	0x10E
-	0x10F-0x13F

Table 31: EEPROM Memory for Common Parameters

Gain 0 data set	Address
EDAC_Y_G0	0x140
EDAC_X_G0	0x141
EDAC_Z_G0	0x142
ESENS_Y_G0	0x143
ESENS_X_G0	0x144
ESENS_Z_G0	0x145
ESENS_TC_Y_G0	0x146
ESENS_TC_X_G0	0x147
ESENS_TC_Z_G0	0x148
EOFFSET_Y_G0	0x149
EOFFSET_X_G0	0x14A
EOFFSET_Z_G0	0x14B
EOFFSET_TC_Y_G0	0x14C
EOFFSET_TC_X_G0	0x14D
EOFFSET_TC_Z_G0	0x14E
-	0x14F

Gain 1 data set	Address
EDAC_Y_G1	0x150
EDAC_X_G1	0x151
EDAC_Z_G1	0x152
ESENS_Y_G1	0x153
ESENS_X_G1	0x154
ESENS_Z_G1	0x155
ESENS_TC_Y_G1	0x156
ESENS_TC_X_G1	0x157
ESENS_TC_Z_G1	0x158
EOFFSET_Y_G1	0x159
EOFFSET_X_G1	0x15A
EOFFSET_Z_G1	0x15B
EOFFSET_TC_Y_G1	0x15C
EOFFSET_TC_X_G1	0x15D
EOFFSET_TC_Z_G1	0x15E
-	0x15F

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland

Gain 2 data set	Address
EDAC_Y_G2	0x160
EDAC_X_G2	0x161
EDAC_Z_G2	0x162
ESENS_Y_G2	0x163
ESENS_X_G2	0x164
ESENS_Z_G2	0x165
ESENS_TC_Y_G2	0x166
ESENS_TC_X_G2	0x167
ESENS_TC_Z_G2	0x168
EOFFSET_Y_G2	0x169
EOFFSET_X_G2	0x16A
EOFFSET_Z_G2	0x16B
EOFFSET_TC_Y_G2	0x16C
EOFFSET_TC_X_G2	0x16D
EOFFSET_TC_Z_G2	0x16E
-	0x16F

Gain 3 data set	Address
EDAC_Y_G3	0x170
EDAC_X_G3	0x171
EDAC_Z_G3	0x172
ESENS_Y_G3	0x173
ESENS_X_G3	0x174
ESENS_Z_G3	0x175
ESENS_TC_Y_G3	0x176
ESENS_TC_X_G3	0x177
ESENS_TC_Z_G3	0x178
EOFFSET_Y_G3	0x179
EOFFSET_X_G3	0x17A
EOFFSET_Z_G3	0x17B
EOFFSET_TC_Y_G3	0x17C
EOFFSET_TC_X_G3	0x17D
EOFFSET_TC_Z_G3	0x17E
-	0x17F

Table 32: EEPROM Memory for Gain Dependent Settings

Table 33 shows the memory content after the gain dependent settings until the last address where the checksum is expected. To activate the EEPROM data, so that all settings contained in it are loaded to the respective registers at power-up, address 0x1FE must contain the key data 0xA5 (165) and address 0x1FF must contain the valid checksum.
A valid checksum means, that the two's complement sum of all data bytes stored in the entire EEPROM (including the checksum) equals 0. The following algorithm details the checksum calculation:

1: tmp_value = (sum of data from address 0x100 to 0x1FE) modulo 256
2: checksum = 256 – tmp_value

-	0x180-0x1FD
KEY	0x1FE
CHECKSUM	0x1FF

Table 33: Memory Map with Checksum and Key

PHONE +41 43 205 26 37
FAX +41 43 205 26 38
E-MAIL info@senis.ch
SENIS AG
Neuhofstrasse 5a
6340 Baar, Switzerland